

**Amendments to the Specification:**

Please amend paragraph number [0003] as follows:

[0003] The semiconductor industry is in the midst of a movement toward greater integrated circuit densification and miniaturization. Resulting from this movement is the development of highly compact and efficient semiconductor devices, attended by an increase in the complexity and number of such semiconductor devices that can now be successfully aggregated on a single integrated circuit wafer. These benefits ~~have in turn~~ have, in turn, resulted in the availability of more compact and efficient integrated circuits, and in the lower cost of these integrated circuits.

Please amend paragraph number [0009] as follows:

[0009] As PLAD is not highly selective of the atoms being driven into ~~silicon~~ semiconductor substrate 10, heavier atoms within a carrier gas are driven into ~~silicon~~ semiconductor substrate 10 with a greater force than dopant atoms, and are consequently driven to a greater depth. This inconsistency in depth causes a jagged unevenness to bottom component 16a of junctions 16. Junctions 16 also have a dopant concentration gradient that terminates abruptly at ~~edges~~ bottom component 16a. The abrupt dopant concentration gradient termination, together with unevenness of bottom component 16a, cause an undesirable increase in reverse bias current leakage. Reverse bias current leakage causes a drain of power through the integrated circuit when finished, a problem which is at odds with the low power requirements of modern integrated circuit applications.

Please amend paragraph number [0011] as follows:

[0011] One method used in the prior art for solving the problem of excessive junction underlap has been to form polysilicon spacers on the sides of the gate ~~region~~ region 14 at the periphery thereof, such as spacers 18 of Figure 2. Spacers 18 are formed by conventional processes at the edge of gate region 14 prior to PLAD. Spacers 18 further the distance between junctions 16 and prevent junction underlap below gate region 14, thus maintaining a low threshold voltage. Nevertheless, the use of spacers 18 does not solve the problems of reverse

bias current leakage. The formation of spacers also adds processing steps and thus throughput time to the integrated circuit formation process.

Please amend paragraph number [0014] as follows:

[0014] ~~It is an object of the~~ The present invention relates to ~~provide~~ a method of forming shallow, heavily doped junctions on silicon substrates of integrated circuit wafers in order to provide smaller, more efficient transistors, diodes, resistors, and other semiconductor devices.

Please amend paragraph number [0015] as follows:

[0015] ~~It is another object of the~~ The present invention also relates to ~~provide such a~~ method of forming shallow junctions which utilizes PLAD.

Please amend paragraph number [0016] as follows:

[0016] ~~It is further an object of the~~ The present invention also relates to ~~provide such a~~ method which remedies rough and jagged unevenness of the bottom component of the junctions, abrupt dopant concentration gradient termination of the junctions, and high reverse bias current leakage which ~~result~~ results from PLAD formation of junctions.

Please amend paragraph number [0017] as follows:

[0017] To achieve the foregoing ~~objects, and~~ advantages and, in accordance with the invention as embodied and broadly described herein in the preferred embodiment, a method is provided for forming a shallow junction with a variable profile gradation of dopants.

Please amend paragraph number [0018] as follows:

[0018] ~~The first step of the~~ The method of the present invention comprises providing a semiconductor wafer having a surface on which to form the shallow junction. In one embodiment, the surface comprises a silicon substrate of an in-process integrated circuit wafer and the junction being formed comprises one of a source or a drain of a MOS transistor.

Please amend paragraph number [0019] as follows:

[0019] ~~A further step comprises conducting a~~ PLAD operation is conducted to form a shallow, highly doped inner portion of the junction having a high concentration of dopants.

Please amend paragraph number [0020] as follows:

[0020] ~~A further step comprises conducting a~~ second doping operation is conducted to form a lightly doped outer portion of the junction. In one embodiment, ~~this step~~ the doping comprises a conventional ion bombardment implantation doping operation with low power and low dopant dosage. The conventional ion bombardment implantation doping operation is typically conducted with a medium power implanter. The result of the conventional ion bombardment implantation doping operation is a lightly doped outer portion surrounding a heavily doped inner portion. The lightly doped outer portion has a bottom edge that is more even and straight than edges of junctions formed by PLAD. The lightly doped outer portion also has a lower concentration of dopants than the heavily doped inner portion.

Please amend paragraph number [0021] as follows:

[0021] ~~Another step of the method of the present invention is to anneal the~~ The semiconductor wafer is then annealed. The anneal causes a more even distribution of dopant concentration therein and helps to remove imperfections in the internal lattice structure. ~~The~~ This anneal is ~~an optional step that~~ and can be conducted after each doping operation, or after any of the doping operations.

Please amend paragraph number [0026] as follows:

[0026] In order that the manner in which the above-recited and other advantages ~~and~~ ~~objects~~ of the invention are obtained will be understood, a more particular description of the invention briefly described above will be rendered by reference to specific embodiments thereof which are illustrated in the appended drawings. Understanding that these drawings depict only typical embodiments of the invention and are ~~not therefore~~ not, therefore, to be considered

limiting of its scope, the invention will be described and explained with additional specificity and detail through the use of the accompanying drawings, which will be briefly described below.

Please amend paragraph number [0027] as follows:

[0027] Figure 1 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a step of a conventional PLAD process of the prior-art. art;

Please amend paragraph number [0028] as follows:

[0028] Figure 2 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a further step of the prior art PLAD process from that depicted in ~~Figure 1.~~ Figure 1;

Please amend paragraph number [0029] as follows:

[0029] Figure 3 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a step of the method of the present ~~invention.~~ invention;

Please amend paragraph number [0030] as follows:

[0030] Figure 4 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a further step of the method of the present invention from that depicted in ~~Figure 3.~~ Figure 3;

Please amend paragraph number [0031] as follows:

[0031] Figure 5 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a step of an ~~alternate~~ alternative embodiment of the method of the present ~~invention.~~ invention; and

Please amend paragraph number [0032] as follows:

[0032] Figure 6 is a cross-sectional depiction of a portion of an in-process integrated circuit wafer showing the results of a further step of the ~~alternate~~ alternative embodiment of the method of the present invention from that depicted in Figure 5.

Please amend paragraph number [0035] as follows:

[0035] In forming the partially completed gate structure of Figure 3, gate oxide layer 22 is formed over silicon substrate 20. A gate region 24, which is formed over silicon ~~substrate 10~~ substrate 20 and gate oxide layer 22, leaves exposed portions of silicon substrate 20 on which junctions will be formed.

Please amend paragraph number [0036] as follows:

[0036] The next step in the method of the present invention comprises conducting a PLAD operation to dope the exposed portion of silicon substrate 20, producing highly doped inner portions 26 having a depth of less than about 1000 angstroms. The PLAD operation is conducted in an energy range of about 5 KeV to about 15 KeV. Highly doped inner portions 26 will preferably be doped to a dopant concentration range of about  ~~$1 \times 10^{19}$~~   $1 \times 10^{19}$  to about  ~~$5 \times 10^{21}$~~   $5 \times 10^{21}$  atoms per  ~~$\text{cm}^3$~~   $\text{cm}^3$ . Any common dopant, such as boron or phosphorus, can be doped into silicon substrate 20. PLAD process machines are available from Varian Associates of Palo ~~Alto~~ Alto, California, USA.

Please amend paragraph number [0037] as follows:

[0037] The PLAD operation is followed with a conventional ion bombardment implantation doping operation using dopants of the same type as were used for the PLAD operation. The conventional ion bombardment implantation doping operation is conducted without a plasma. Preferably, the conventional ion bombardment implantation doping operation is conducted at the higher energy range of between about 10 KeV and about 25 KeV using a medium current implanter. A medium current implanter is an implanter which operates in an

energy range of about 0 to about 200 KeV, such as the E500 manufactured by Varian Associates of Palo-Alto Alto, California, USA.

Please amend paragraph number [0038] as follows:

[0038] The conventional ion bombardment implantation doping operation results in a set of junctions 30 with lightly doped outer portions 28 which extend to a greater depth than highly doped inner portions 26, and which have a lower concentration of dopants than highly doped inner portions 26. The concentration of dopants of lightly doped outer portions 28 is preferably in a range of about ~~1x10<sup>16</sup>~~ 1 x 10<sup>16</sup> to about ~~1x10<sup>19</sup>~~ 1 x 10<sup>19</sup> atoms per ~~cm<sup>3</sup>~~ cm<sup>3</sup>. Each of lightly doped outer portions 28 preferably will circumscribe and extend below and beyond ~~a corresponding~~ corresponding highly doped inner portions 26 by a depth in a range of about 250 angstroms to about 750 angstroms. The conventional ion bombardment implantation doping operation step will increase the dopant concentration in highly doped inner portions 26, and will also create lightly doped outer portions 28.

Please amend paragraph number [0042] as follows:

[0042] The structure of Figure 4 also produces a less abrupt, more ~~tailored~~ tailored, doping concentration gradation with a variable dopant concentration profile which has been found to reduce reverse bias current leakage. Thus, the use of PLAD allows the formation of a shallow junction with a high dopant concentration close to the surface of silicon substrate 20, which helps to subsequently form lower resistance contacts and interconnects superadjacent thereto, while the method of the present invention eliminates the aforementioned problems with conventional PLAD processes.

Please amend paragraph number [0044] as follows:

[0044] In the embodiment where the conventional ion bombardment implantation operation is conducted first, a thin oxide layer can be formed over gate region 24 and junction 30 prior to the PLAD operation and after the conventional ion bombardment implantation operation. By way of example, a TEOS (tetraethylorthosilicate) layer ~~34~~ 34, as seen in ~~Figure 5~~ Figure 5, is

formed, preferably having a thickness in a range of about 50 to about 100 angstroms. The PLAD operation is then conducted through TEOS layer 34, such that the structure of Figure 6 results. When so doing, TEOS layer 34 serves as an implant barrier to the PLAD operation. The use of TEOS layer 34 as an implant barrier further reduces the depth of highly doped inner portions 26 while maintaining the depth of lightly doped outer portions 28. The use of thin gate oxide layer 22 as an implant barrier also maintains the high concentration of dopants on the surface of junctions ~~30,~~ 30 for subsequent formation of a low resistance contact and interconnect interface.

Please amend paragraph number [0048] as follows:

[0048] The method of the present invention may be embodied in other specific forms without departing from its spirit or essential characteristics. The described embodiments are to be considered in all respects only as ~~illustrated~~ illustrative and not restrictive. The scope of the invention is, therefore, indicated by the appended claims rather than by the foregoing description. All changes which come within the meaning and range of equivalency of the claims are to be embraced within their scope.